What is claimed is:

1. A semiconductor memory device, comprising:

a plurality of memory banks; and

a plurality of control pads and a plurality of I/O (input/output) pads for reading data from and writing data in the memory banks, wherein the plurality of control pads and I/O pads are disposed in a region between adjacent memory banks and in a peripheral region surrounding the memory banks.

2. The device of claim 1, wherein the plurality of control pads are sequentially arranged in the region between adjacent memory banks.

3. The device of claim 1, wherein the plurality of I/O pads are arranged in the peripheral region surrounding the memory banks.

4. A semiconductor memory device, comprising:

a plurality of memory banks arranged at a cell region of a memory chip; and

a plurality of control pads and a plurality of I/O (input/output) pads, separately arranged from each other at the memory chip, for reading data from and writing data in the memory banks, wherein the plurality of control pads are sequentially arranged in a region between adjacent memory banks of the memory chip and the plurality of I/O pads are dispersed in a peripheral region surrounding the memory banks.

5. A semiconductor memory device, comprising:

a plurality of memory banks arranged at a cell region of a memory chip; and

a plurality of control pads and a plurality of I/O (input/output) pads for reading data from and writing data in the plurality of memory banks, wherein the plurality of control pads are sequentially arranged in a region between adjacent memory banks and are commonly shared by the plurality of memory banks, and wherein a predetermined number of I/O pads of the plurality of I/O pads are arranged in a periphery region surrounding the memory banks and the plurality of I/O pads are commonly shared by the plurality of memory banks.

6. A semiconductor memory device, comprising:

a plurality of memory banks arranged at a cell region of a memory chip, each of the plurality of memory banks comprising a plurality of bank areas;

a plurality of control pads that are sequentially arranged in a region between adjacent memory banks and are commonly shared by the memory banks; and

a plurality of I/O pads that are arranged in a peripheral region surrounding the memory banks and are commonly shared by memory banks.

7. The device of claim 6, wherein the number of bank areas comprising each memory bank corresponds to the number of memory banks, and wherein the data corresponding to one of the bank areas is read from and written in the corresponding bank area of each of the plurality of memory banks.

8. The device of claim 6, wherein a predetermined number of the plurality I/O pads are allocated to each of the memory banks, and wherein the predetermined number of I/O pads allocated for a corresponding memory bank are disposed near the corresponding memory bank in the peripheral region surrounding the memory banks, and wherein the data stored or data to be stored in one of the plurality of memory banks is read from or written in the corresponding one of the memory banks through the I/O pads allocated to the corresponding memory bank.

9. The device of claim 8, wherein the data stored or the data to be stored in one of the plurality of memory banks is read from or written in the corresponding one of each of the bank areas of the memory banks through the plurality of control pads.

10. A semiconductor memory device, comprising:

a plurality of memory banks arranged at a cell region of a memory chip; and

a plurality of control pads and a plurality of I/O (input/output) pads for reading data from and writing data in the memory banks,

wherein each of the plurality of memory banks comprises a plurality of bank areas, wherein the number of bank areas corresponds to the number of the plurality of memory banks and the data corresponding to one of the plurality of bank areas is read from or written in the corresponding bank area of each of the memory banks,

wherein the plurality of control pads are sequentially arranged in a region between adjacent memory banks and are commonly shared by the plurality of memory banks,

wherein the plurality of I/O pads are arranged in a peripheral region surrounding the memory banks and are commonly shared by the plurality of memory banks, and

wherein a predetermined number of I/O pads are allocated to the outer potion of each of the memory banks.

11. A method for driving data in a semiconductor memory device comprising a plurality of memory banks arranged at a cell region of a memory chip, each of the memory banks comprising a plurality of bank areas in which the number of bank areas corresponds to the number of the memory banks, a plurality of control pads sequentially arranged in a region between adjacent memory banks of the memory chip, and a plurality of I/O pads arranged in a peripheral region surrounding the memory banks, in which a predetermined number of I/O pads are allocated to each memory bank and are disposed near the corresponding memory bank in the perpherial region surrounding the memory banks, the method comprising the steps of:

writing data to be stored in a bank area of a memory bank through the plurality of control pads and the predetermined number of I/O pads allocated to the corresponding memory bank; and

reading data stored in a bank area of a memory bank through the plurality of control pads and the predetermined number of I/O pads allocated to the corresponding memory bank.